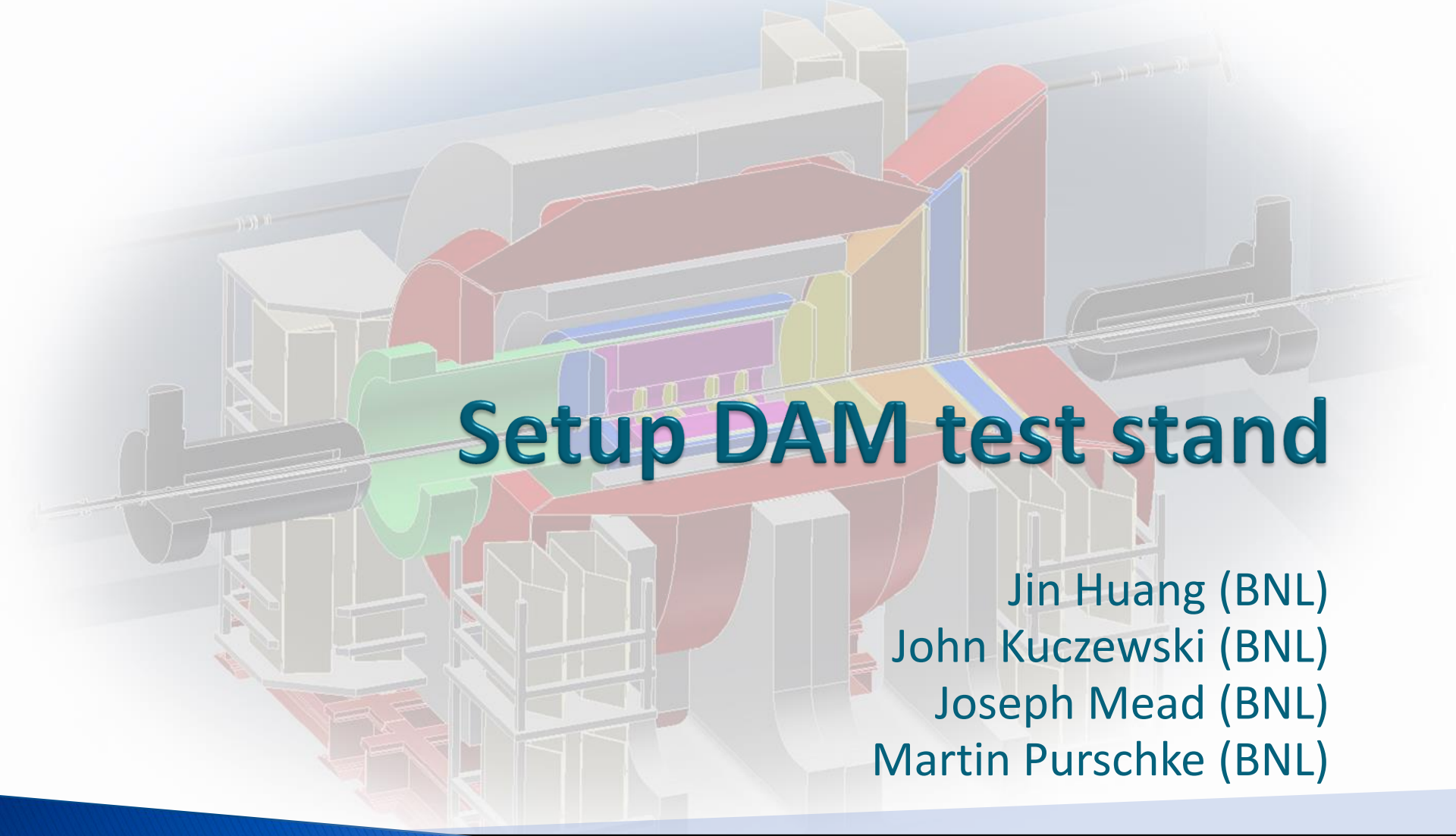


Setup DAM test stand

Jin Huang (BNL)
John Kuczewski (BNL)
Joseph Mead (BNL)
Martin Purschke (BNL)

PHENIX

Goals of setting up a test stand

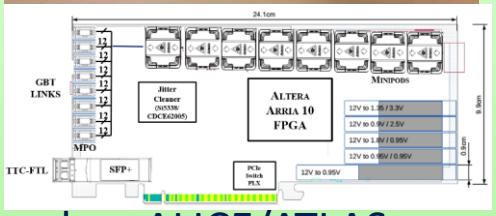
- Gain experience with operating a FELIX PCIe board
- Demonstrate 4 Gbps bi-directional optical link, FEE <-> FELIX PCIe board (8b10b encoding)
  - Downlink should deliver 9.4 MHz Beam Collision Clock (BCO)
  - Downlink should deliver a synchronization signal to synchronize FEE and FELIX BCO counter after reset
  - Downlink should allow deliver slow control command packages
  - Uplink should deliver emulated data package at peak rate of ~2 Gbps (+ snow control reply packages)
- Demonstrate top level FPGA design and resource counting
- Demonstrate FPGA -> PCIe -> DMA rate (already demonstrated by ATLAS group)
- Demonstrate CPU-based LZO data compression speed (60 MB/s/core) and compression ratio (~60%?) using emulated data. (can be done at generic server elsewhere)
- Target delivery date: Apr 2017, CD-1 review practice

Reminder: Full DAM system concept

Data Aggregation Module (DAM):
PCIex8 or x16 card with multiple (8-48x) GBT fiber IO

Option 1: ATLAS FELIX

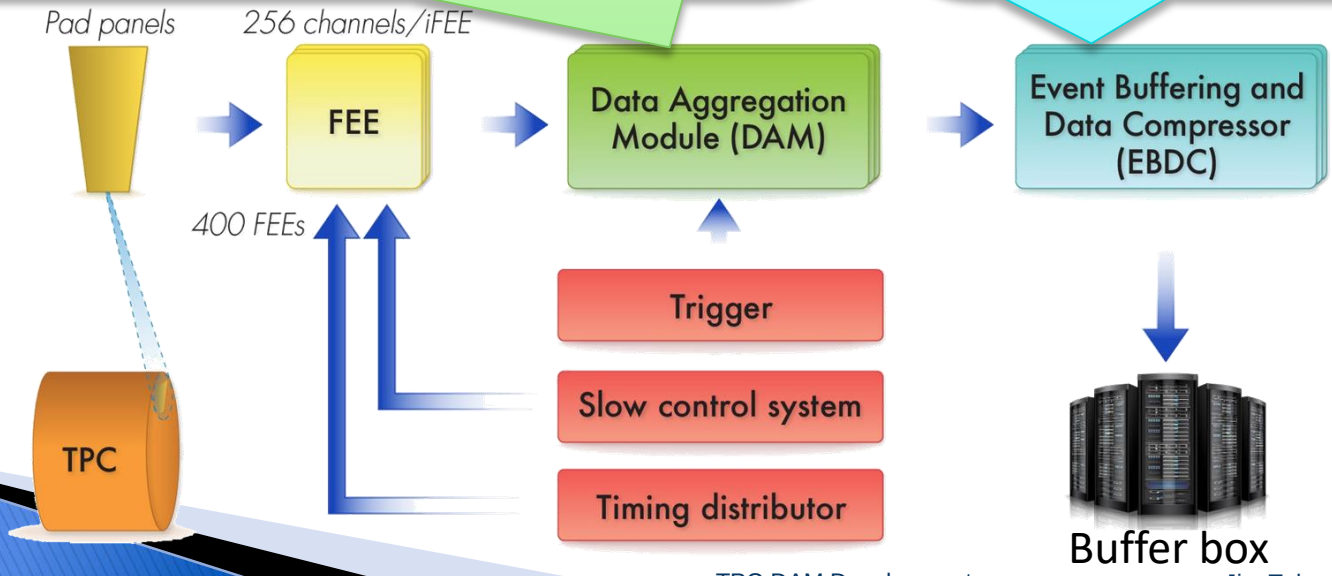
Option 2:LHCb/ALICE CRU



~~Option 3: build our own based on ALICE/ATLAS exp.~~

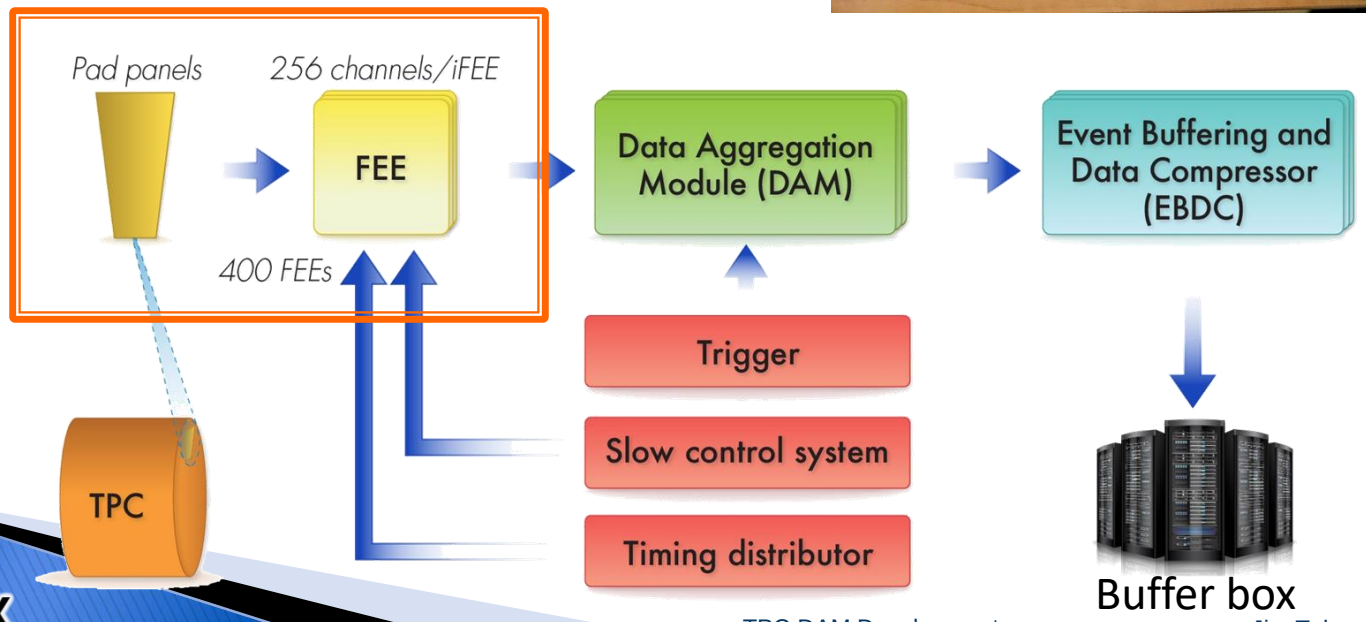
Event Buffering and Data Compressor (EBDC): Rack server that can host at 1x PCIex16 cards + 2x 10 Gbps Ethernet port

Example: Dell PowerEdge R830
12 cores, 1x10 GBps, ~ 5k$



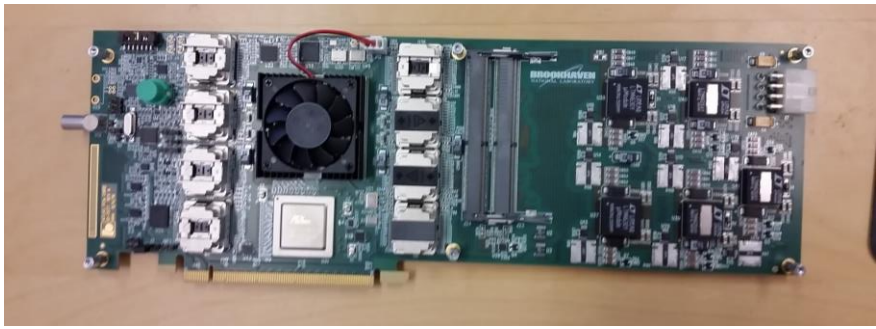
Assembly of a DAM test stand : FEE emulator

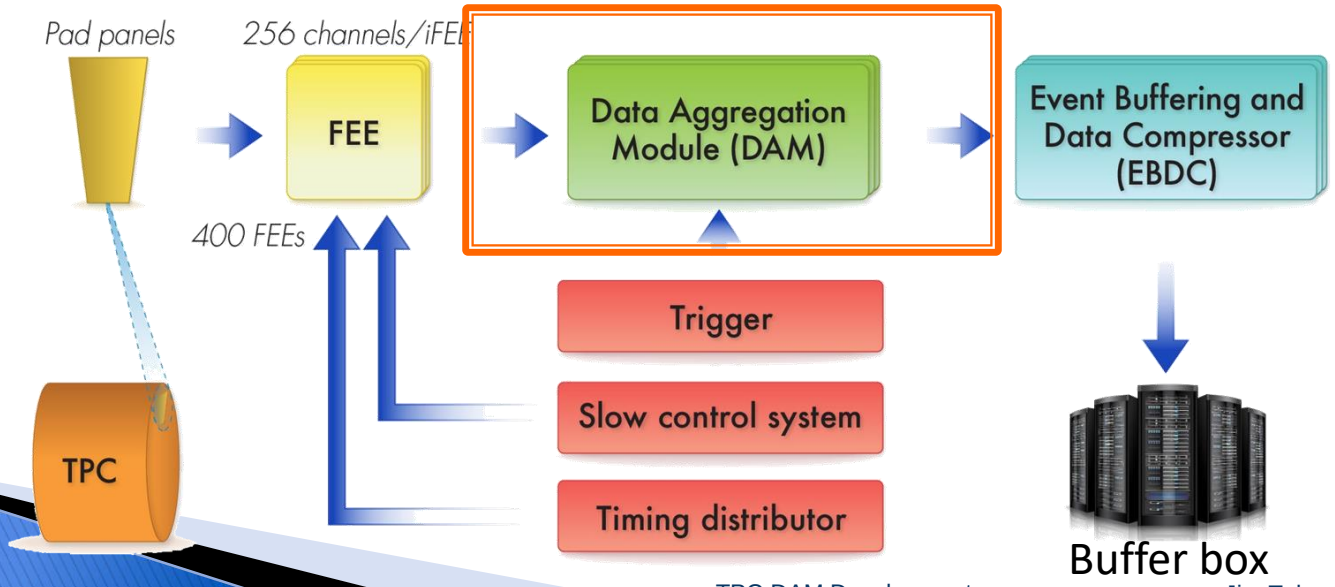
- Xilinx Atrix-7 XC7A200T evaluation board
- 8x SPF mezzanine card (from John)



Assembly of a DAM test stand : DAM card

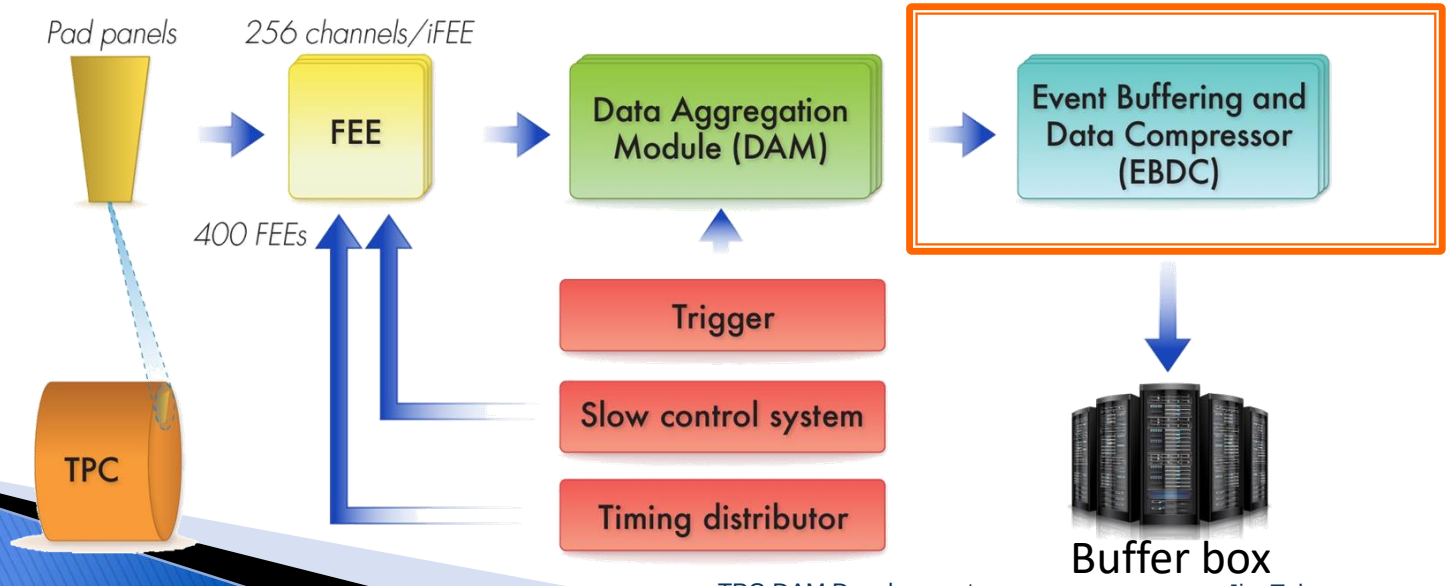
- Request borrow one version 1.5 FELIX PCIe card
- Main improvement in v1.5 is clock jitter cleaner? - yes
- Use internal clock that approximately 9.4 Mhz to emulate sPHENIX BCO
- MTP cable and MTP/MPO cassette





Assembly of a DAM test stand : EBDC Server

- Martin Purschke kindly provided a server to use the test stand
- Asus M5A88-M mother board
  - One PCIe x16
  - Seems has a [AMD/ATI] SBx00 SMBus Controller
- Need to verify SMBus support



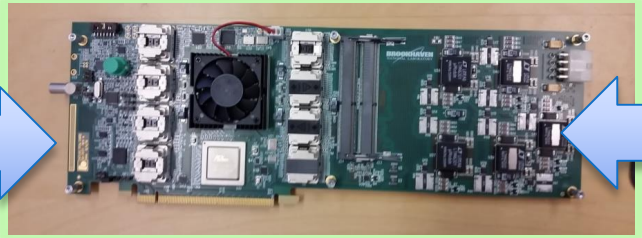
Assembly of a DAM test stand

Xilinx Atrix-7 XC7A200T + 8x SFP

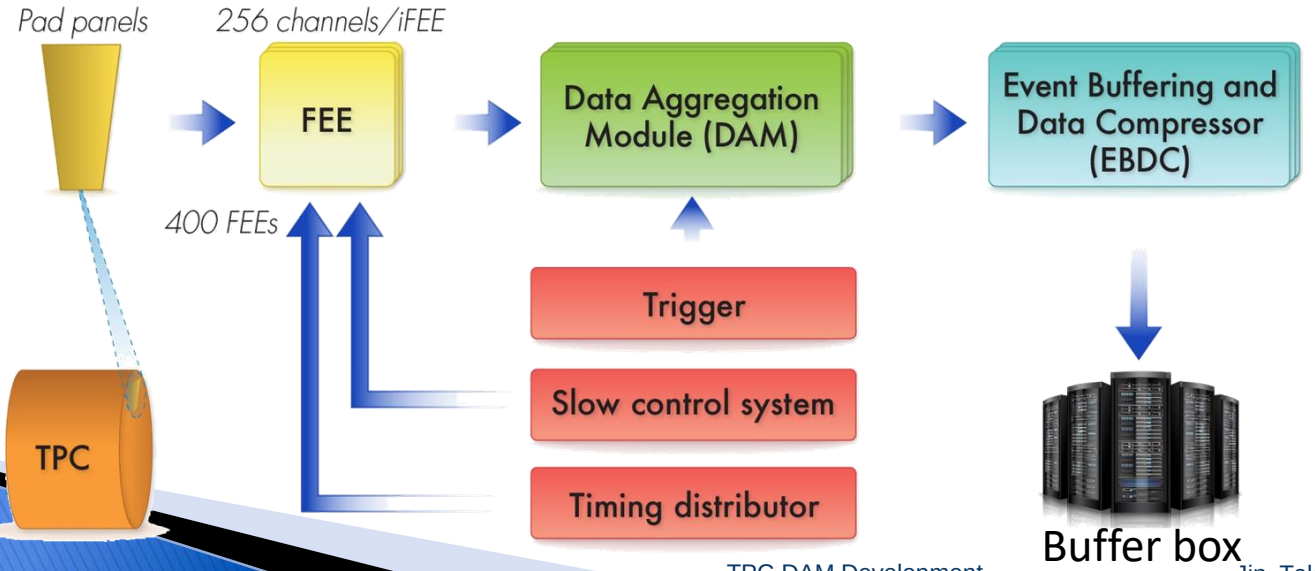
Requesting a FELIX v1.5 PCIe card

A server

MTP/MPO



PCIex16
SMB(?)



Extra discussion with ATLAS experts

- If the design is proven sound, we plan to order few more v2.0 FELIX cards in the pre-production batch later 2017
- A generic SFP+ timing mezzanine card might work well for sPHENIX already. Main signals are 9.4 MHz BCO and trigger bits
- sPHENIX MAPS inner tracker group used FELIX card as one option for readout too
  - Default readout option: ALICE CRU/LHCb PCIe40
  - Plan to have a MAPS DAQ discussion some time March 2017
  - Choice may driven by interest of DAQ lead institution (LANL, UT Austin, ...)